PENDING CLAIMS AS AMENDED

Please amend the claims as follows:

1. (Currently Amended) A searcher for finding the frequency of a received signal comprising a phase error, the searcher comprising:

a frequency locked loop that generates a phase increment signal in response to the phase error of the received signal;

a programmable rotator coupled to the frequency locked loop, the programmable rotator performing a phase rotation function ~~in response to the phase increment signal~~;

a phase error accumulator accumulating results of the phase ~~error~~ increment signals from the frequency locked loop and generating a control signal that instructs the programmable rotator to perform the phase rotation function; and

a shift register coupled between the phase error accumulator and the programmable rotator, the shift register truncating a predetermined number of bits of the control signal.

2. (Original) The searcher of claim 1 wherein the programmable rotator is an 8-Phase Shift Keying rotator.

3. (Original) The searcher of claim 1 wherein the programmable rotator is a Quadrature Phase Shift Keying rotator.

4. (Cancelled).

5. (Cancelled)

6. (Cancelled)

7. (Cancelled)

8. (Previously Presented) The searcher of claim 1 wherein the phase error accumulator accumulates phase increment signals over a 64-chip interval.

9. (Previously Presented) The searcher of claim 2 wherein the frequency locked loop further comprises means for generating an initial phase signal that is coupled to the 8-Phase Shift Keying programmable rotator and initializes the 8-Phase Shift Keying programmable rotator to a predetermined starting phase.

10. (Cancelled)

11. (Cancelled)

12. (Cancelled)

13. (Previously Presented) The searcher of claim 3 wherein the frequency locked loop further comprises means for generating an initial phase signal that is coupled to the Quadrature Phase Shift Keying programmable rotator and initializes the Quadrature Phase Shift Keying programmable rotator to a predetermined starting phase.

14. (Cancelled).

15. (Cancelled).

16. (Cancelled).

17. (Cancelled).

18. (Cancelled).

19. (Cancelled).

20. (Cancelled).

21. (Cancelled).

22. (Cancelled).

23. (Cancelled).

24. (Cancelled).

25. (Currently Amended) A searcher for finding the frequency of a received signal comprising a plurality of segments, the searcher comprising:

a first phase rotator configured to phase rotate a signal to partially reduce a phase error of the signal and produce a first phase rotator output signal;

an accumulator configured to accumulate a plurality of chips from the first phase rotator output signal to form segments ~~from~~ of the first phase rotator output signal; ~~and~~

a second rotator configured to phase rotate the segments of the first phase rotator output signal to further reduce the phase error of the signal by adjusting the phase over each segment[~~,~~] ; and

wherein the second rotator is implemented within a frequency locked loop producing a phase increment signal based on the phase error, the first phase rotator configured to phase rotate the signal based on an accumulation of the phase increment signal.

26. (Previously Presented) A searcher in accordance with claim 25, wherein the second rotator is implemented within a frequency locked loop producing a phase increment signal based on the phase error, the first phase rotator configured to phase rotate the signal based on the phase increment signal.

27. (Previously Presented) A searcher in accordance with claim 26, wherein the first phase rotator is configured to partially reduce the phase error by compensating for instantaneous signal phase changes over each segment.

28. (Previously Presented) A searcher in accordance with claim 27, wherein the second phase rotator is configured to partially phase rotate the signal based on an average phase of the signal over multiple segments.

29. (Previously Presented) A searcher in accordance with claim 28, wherein the first phase rotator is a high-speed low-resolution phase rotator and the second phase rotator is a low-speed high-resolution phase rotator.

30. (Previously Presented) A searcher in accordance with claim 29, wherein the first phase rotator is hardware rotator and the second phase rotator is a DSP rotator.

31. (Currently Amended) A method of finding a signal having a deviation from an expected frequency, the method comprising:

first phase rotating a signal to partially reduce a phase error of the signal and produce a partially rotated output signal;

accumulating a plurality of chips from the partially rotated output signal to form segments ~~from~~ of the partially rotated output signal; ~~and~~

second phase rotating the segments of the partially rotated output signal to further reduce the phase error of the signal by adjusting the phase over each segment[~~,~~] ; and

generating a phase increment signal based on the phase error, the first phase rotating the signal to partially reduce the phase error based on an accumulation of the phase increment signal.

32. (Previously Presented) A method in accordance with claim 31, further comprising:

generating a phase increment signal based on the phase error, the phase rotating the signal to partially reduce the phase error based on the phase increment signal.

33. (Previously Presented) A method in accordance with claim 32, wherein the phase rotating the signal to partially reduce the phase error comprises compensating for instantaneous signal phase changes over each segment.

34. (Previously Presented) A method in accordance with claim 33, wherein the phase rotating the signal to further reduce the phase error comprises compensating for instantaneous signal phase changes over each segment by partially phase rotating the signal based on an average phase of the signal over multiple segments.